CLAIMS

1. A variable power regulator, comprising:

a pulse modulator generating a pulse signal having a pulse width; and

a phase delay array receiving said pulse signal and a frequency selection signal, and generating a plurality of phased burst signals, each having a frequency determined by said frequency selection signal wherein at least two of said phased burst signals have different start times.

2. A circuit as claimed in claim 1, wherein each said phased burst signal of said plurality of phased burst signals regulates a respective load.

3. A circuit as claimed in claim 1, wherein said pulse modulator includes a variable selector for selecting said pulse width.

4. A circuit as claimed in claim 3, wherein said variable selector comprises a dimmer providing a DC signal, and an oscillator generating a triangular waveform, wherein said pulse width being determined by the intersection of said DC signal and said triangular waveform.

5. A circuit as claimed in claim 4, wherein said dimmer further comprising a dim selector for setting the DC value of said DC signal, and a polarity selector for determining the section, of said intersection of said DC signal and said triangular waveform, to be used for generating the pulse width of said pulse width modulated signal.

6. A circuit as claimed in claim 1, further comprising a frequency selector receiving a reference signal and generating said frequency selection signal based on said reference signal, wherein said phase delay array receiving said frequency selection signal and setting the frequency of said pulse signal to said frequency selection signal.

7. A circuit as claimed in claim 1, wherein said phase delay array includes a counter for timing each said phased burst signal of said plurality of phased burst signals such that at least two of said phased burst signals have different start times.

8. A circuit as claimed in claim 1, wherein each said phased burst signal has a pulse width equal to said pulse width of said pulse signal.

9. A circuit as claimed in claim 1, wherein said phase delay array includes a phase delay generator for generating at least one phase delay value.

10. A circuit as claimed in claim 9, wherein said at least one phase delay value is a constant.

11. A circuit as claimed in claim 1, wherein said phase delay array includes at least one select signal input for determining the number of said phased burst signals to generate.

12. A circuit as claimed in claim 1, further comprising at least one phase array driver receiving at least one said phased burst signal and generating at least one respective power regulating signal for at least one respective load, said power regulating signal having a phase value equal to the phase value of said phased burst signal.

13. A circuit as claimed in claim 12, wherein each phase array driver receives two said phased burst signals which are 180° out of phase and generates two respective power regulating signals which are 180° out of phase.

14. A circuit as claimed in claim 12, wherein said phase array driver further comprising soft start circuitry generating power to said at least one respective load during a soft start period, wherein a soft start period defining a period wherein said at least one load is powered from an OFF state to an operationally ON state; and wherein once said load is at least at an operationally ON state, power to said load is regulated by said respective phased burst signal during a burst mode period.

15. A circuit as claimed in claim 12, wherein said phase array driver further comprising at least one comparator for limiting voltage of said at least one load to a predetermined voltage.

16. A circuit as claimed in claim 14, wherein said phase array driver including at least one error amplifier, receiving a feedback from said load during said soft start period, and further, receiving feedback from said at least one phased burst signal, wherein said error amplifier generates said at least one respective power regulating signal.

17. A circuit as claimed in claim 12, wherein said phase array driver further comprising at least one current or voltage feedback selector for selecting either to regulate current to said at least one respective load or regulate the voltage of said at least one respective load.

18. A circuit as claimed in claim 17, wherein said at least one current or voltage feedback selector comprises a multiplexer.

19. A circuit as claimed in claim 14, wherein said phase array driver further comprising a selector for selecting either said soft start period or said burst mode period.

20. A circuit as claimed in claim 19, wherein said selector comprises a multiplexer.

21. A circuit as claimed in claim 12, wherein said phase array driver further comprising a minimum voltage selector to regulate power to said at least one respective load with a selected current or minimum voltage.

22. A circuit as claimed in claim 21, wherein said selector comprises a multiplexer.

23. A circuit as claimed in claim 12, wherein said phase array driver further comprising a ramp circuit to deliver power to said at least one load.

24. A circuit as claimed in claim 12, wherein said phase array driver further comprising a DC/AC converter circuitry for generating an AC signal for at least one respective load.

25. A circuit as claimed in claim 24, wherein said converter includes a transformer for delivering a high voltage to said load based on said AC signal.

26. A circuit as claimed in claim 12, wherein said phase array driver further comprising protection circuitry for under voltage lock out.

27. A method for generating phase shifted burst mode signals, comprising the steps of:

generating a pulse signal having a pulse width;

generating a frequency selection signal;

generating a plurality of phased burst signals having a frequency of said frequency selection signal and said pulse width of said pulse signal; and

delaying at least one of said phased pulse signals to have a different start time than at least one other of said phased burst signals.

28. A method as claimed in claim 27, further comprising the step of:

regulating power to a plurality of loads using said plurality of said phased burst signals, respectively.

29. A method as claimed in claim 27, further comprising the step of:

generating a constant phase delay between each said phased burst mode signal.

30. A method as claimed in claim 28, wherein said step of generating a constant phase delay between each said phased burst mode signal comprising the step of dividing the period of said frequency selection signal by the number of loads utilized in said plurality of loads to generate a value for said constant phase delay.

31. A phased burst mode dimming system, comprising:

a pulse width modulator generating a pulse width modulated signal;

a variable selector for selecting the width of said pulse width modulated signal; and

a phase delay array receiving said pulse modulated signal and said frequency selection signal, and generating a plurality of phased burst signals by generating a phase delay between at least two said pulse width modulated signals.

32. A circuit as claimed in claim 31, wherein said variable selector comprises a dimmer providing a DC signal, and an oscillator generating a triangular waveform, wherein said pulse width being determined by the intersection of said DC signal and said triangular waveform.

33. A circuit as claimed in claim 32, wherein said dimmer further comprising a dim selector for setting the DC value of said DC signal, and a polarity selector for determining the section, of said intersection of said DC signal and said triangular waveform, to be used for generating the pulse width of said pulse width modulated signal.

34. A circuit as claimed in claim 31, further comprising a frequency selector receiving a reference signal and generating a frequency selection signal, wherein said phase delay array receiving said frequency selection signal and setting the frequency of said pulse signal to said frequency selection signal.

35. A circuit as claimed in claim 31, wherein said phase delay array includes a counter for timing each said phased burst signal of said plurality of phased burst signals such that at least two of said phased burst signals have different start times.

36. A circuit as claimed in claim 31, wherein each said phased burst signal has a pulse width equal to said pulse width of said pulse signal.

37. A circuit as claimed in claim 31, wherein said phase delay array includes a phase delay generator for generating at least one phase delay value.

38. A circuit as claimed in claim 37, wherein said at least one phase delay value is a constant.

39. A circuit as claimed in claim 31, wherein said phase delay array includes at least one select signal input for determining the number of said phased burst signals to generate.

40. A circuit as claimed in claim 31, further comprising at least one phase array driver receiving at least one said phased burst signal and generating at least one respective power regulating signal for at least one respective load, said power regulating signal having a phase value equal to the phase value of said phased burst signal.

41. A circuit as claimed in claim 40, wherein each phase array driver receives two said phased burst signals which are 180° out of phase and generates two respective power regulating signals which are 180° out of phase.

42. A circuit as claimed in claim 40, wherein said phase array driver further comprising soft start circuitry generating power to said at least one respective load during a soft start period, wherein a soft start period defining a period wherein said at least one load is powered from an OFF state to an operationally ON state; and wherein once said load is at least at an operationally ON state, power to said load is regulated by said respective phased burst signal.

43. A circuit as claimed in claim 40, wherein said phase array driver further comprising a comparator for limiting voltage of said at least one load to a predetermined voltage.

44. A circuit as claimed in claim 42, wherein said phase array driver further comprising at least one error amplifier, receiving a feedback from said load during said soft start period, and further, receiving feedback from said at least one phased burst signal, wherein said error amplifier generates said at least one respective power regulating signal.

45. A circuit as claimed in claim 40, wherein said phase array driver further comprising at least one current or voltage feedback selector for selecting either to regulate current to said at least one respective load or regulate the voltage of said at least one respective load.

46. A circuit as claimed in claim 42, wherein said at least one current or voltage feedback selector comprises a multiplexer.

47. A circuit as claimed in claim 42, wherein said phase array driver further comprising a selector for selecting either said soft start period or said burst mode period.

48. A circuit as claimed in claim 42, wherein said at least one burst mode selector comprises a multiplexer.

49. A circuit as claimed in claim 40, wherein said phase array driver further comprising a minimum voltage selector to regulate power to said at least one respective load with a selected current or minimum voltage.

50. A circuit as claimed in claim 49, wherein said selector comprises a multiplexer.

51. A circuit as claimed in claim 40, wherein said phase array driver further comprising a ramp circuit to deliver power to said at least one load.

52. A circuit as claimed in claim 40, wherein said phase array driver further comprising a DC/AC converter circuit generating an AC signal to supply power to at least one respective load.

53. A circuit as claimed in claim 52, wherein said converter includes a transformer for delivering high voltage to said load based on said AC signal.

54. A circuit as claimed in claim 40, wherein said phase array driver further comprising protection circuitry for under voltage lock out.

55. A circuit as claimed in claim 6, wherein said frequency selector comprises a frequency doubler, doubling the frequency of said reference signal, and generating said frequency selection signal having a period twice that of said reference signal.

56. A circuit as claimed in claim 34, wherein said frequency selector comprises a frequency doubler, doubling the frequency of said reference signal, and generating said frequency selection

signal having a period twice that of said reference signal.